University of Computer Studies, Yangon
B.C.Sc./B.C.Tech.

CST-301	**: Data and Computer Communications**	**First Semester**
Text book	: Structured Computer Organization (6th Edition) By Andrew S. Tanenbaum. Todd Austin	
Period	**: 45** periods for 15 weeks (3 periods/week)	

Course Description:

Computer design fundamentals for computer technology, Von Neumann computer architecture: processor, memory and I/O. Processor organization: registers, ALU, and control. Memory organization and memory bus, I/O organization: I/O bus, memory mapped I/O. Number representations and ALU designs. Fundamentals of assembly language are used throughout to illustrate concepts. The course provides an accessible introduction to computer hardware and architecture which serve as a useful resource for all computer professionals and engineers who need an overview or introduction to computer architecture. This course takes a modern structured, layered approach to understanding computer systems.

Course Objective:

The objective of this course is to study the internal architecture/components of the computer, how they are integrated together, and the way they are controlled. This course should be preceded by an introduction in Logic and Digital Design. Topics include basic scientific concepts of how data networks function, data transferring techniques starting from hardware levels to high levels of data transferring protocols over intra-networks, and the scientific theories on which the modern digital communication technology is based.

Assessment Plan for the Course

Paper Exam:	70%
Attendance:	10%
Test/ Quiz:	10%
Assessment:	10%

Tentative Lecture Plan

No.	Chapter	Page	Period	Detail Lecture Plan
	Chapter 1 Introduction	1-27	**4**	Lecture + Problems
1	1.1 Structured Computer Organization	1-8	2	Detail explain about languages, levels and Virtual machine

2	1.2 Milestones in Computer Architecture	13-27	1	Assignment & Discussion
3	Problems	52-54	1	No.1,3,7
	Chapter 3 The Digital Logic Level	147-201	**15**	
4	3.1 Gates and Boolean Algebra 3.1.1 Gates 3.1.2 Boolean Algebra 3.1.3 Implementation of Boolean Functions 3.1.4 Circuit Equivalence	147-157	2	Just known Assignment & Discussion
5	3.2 Basic Digital Logic Circuits 3.2.1 Integrated Circuits 3.2.2 Combinational Circuits 3.2.3 Arithmetic Circuits 3.2.4 Clocks	158-169	2	Detail explain
6	3.3 Memory 3.3.2 Flip-Flops 3.3.3 Registers 3.3.4 Memory Organization 3.3.5 Memory Chips	172-180	3	Detail explain
7	3.4 CPU Chips and Buses 3.4.1 CPU Chips 3.4.2 Computer Buses 3.4.3 Bus Width	185-191	3	Detail explain
8	3.4.4 Bus Clocking 3.4.5 Bus Arbitration 3.4.6 Bus Operation	191-201	1 1	Detail explain
9	Problems & Assignments	237-241	2	No.1,13,15,16,17,18,21,24, 25,26,35
10	Tutorial (Chapter 1 and 3)		1	
	Chapter 4 The Micro-architecture level	243-323	**17**	
11	4.1 An Example Micro-architecture 4.1.1 The Data Path 4.1.2 Microinstructions 4.1.3 Microinstruction Control: The Mic-1	243-258	4	Detail explain
12.	4.2 An Example ISA: IJVM 4.2.1 Stacks 4.2.2 The IJVM Memory Model 4.2.3 The IJVM Instruction Set 4.2.4 Compiling Java to IJVM	258-267	3	Detail explain

No.	Chapter	Page	Period	Detail Lecture Plan
13	4.3 An Example Implementation 4.3.1 Microinstructions and Notation 4.3.2 Implementation of IJVM Using the Mic-1	267-282	2	Detail explain
14	4.4 Design Of The Microarchitecture Level 4.4.1 Speed versus Cost 4.4.2 Reducing the Execution Path Length 4.4.3 A Design with Prefetching: The Mic-2 4.4.4 A Pipelined Design; The Mic-3 4.4.5 A Seven-Stage Pipeline: The Mic-4	283-303	2	Detail explain To compare Mic-1. Mic-2, Mic-3 and Mic-4

15	4.5 Improving Performance 4.5.1 Cache Memory 4.5.2 Branch Prediction 4.5.3 Out of Order Execution and Register Renaming 4.5.4 Speculative Execution	303-323	4	Detail Explain
16	Problems and Assignments Tutorial	338-341	1 1	No. 2,5,6,7,10,11
	Chapter 5 The Instruction Set	362-379	**7**	
17	5.3 Instruction Formats 5.3.1 Design Criteria for Instruction Formats 5.3.2 Expanding Opcodes	362-367	2	Detail explain
18	5.4 Addressing 5.4.1 Addressing Modes 5.4.2 Immediate Addressing 5.4.3 Direct Addressing 5.4.4 Register Addressing	371-372	1	Detail explain
19	5.4.5 Register Indirect Addressing 5.4.6 Indexed Addressing 5.4.7 Based-Indexed Addressing 5.4.8 Stack Addressing	373-379	2	Detail explain
20	Problems	431-435	1	No. 5,6,7,10,11,12,14,15
21	Tutorial(Chapter 4 and 5)		1	
22	Revision (Chapter 1,3,4,5)		**2**	